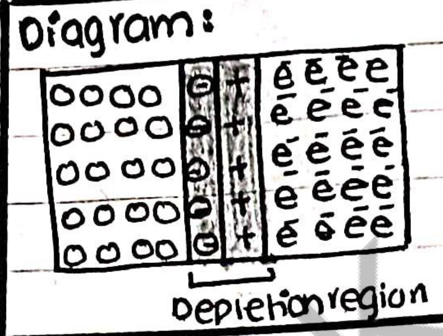
QNO: 1: (a) → BASE IS LIGHTLY DOPED: central region of a transistor is called base which controls flow of charge carriers from Emitter towards the collector.



• **Less Resistance:** Depletion region will be thin of the order of micron (10^{-6} m) due to light doping of base. This will cause its resistance to decrease.

• **Maximum flow of charge carrier:** Due to light doping, majority charge carries flow from emitter to collector.

(b) → COLLECTOR REGION IS LARGER IN SIZE: Collector region collects charge carriers. Due to interaction of charge carriers, collector region heats up and all heat is dissipated.

• **Prevent Overheating:** Collector region is made greater than emitter and base so that heat can dissipate & collector doesn't burn.

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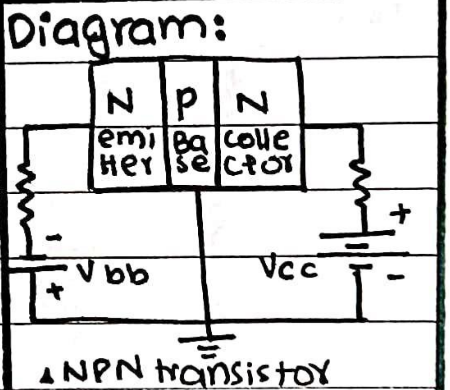
QNO2 → Forward bias: Emitter-Base junction

→ Reverse bias: Collector base junction.

→ Applying voltage: Given that $V_{CC} > V_{BB}$, majority charge carriers flow to collector region from base.



→ Minute base current:

- Base is very lightly doped contributing to very small base current. Base region is very thin of the order of micron (10^{-6} m)
- Vcc is very high potential voltage thus collector current is high.

→ Mathematically:

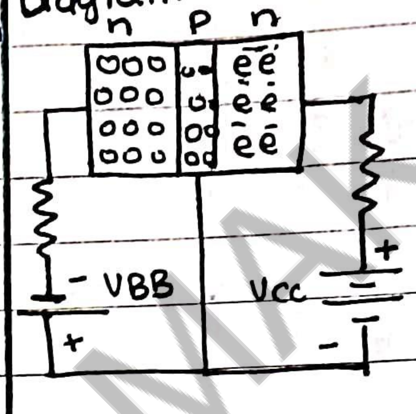
$$I_E = I_B + I_C$$

Majority of I_E is converted into I_C.

QNO 3: →Forward Biasing the Emitter-Base Junction:

This biasing decreases width of depletion region which decreases forward resistance. Hence a large number of charge carriers move from emitter region to base region.

Diagram:



→Reverse Biasing the Collector Base Junction:

This reverse voltage is essential for establishing large collector current.

→When this biasing is reversed: If emitter base junction is reverse biased, depletion region becomes wide causing great hindrance to flow of charge.

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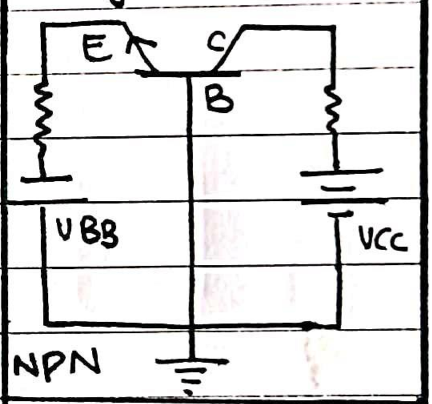
QNO 4: →NPN TRANSISTOR:

•Sandwiched Region: A P-Type region is sandwiched between two N-Type regions.

•Biasing: Forward biased voltage at emitter-base junction VBB will move the free electrons from emitter to base region which are swept toward collector region.

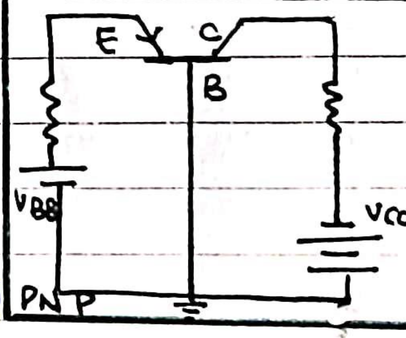
Diagram:



→PNP TRANSISTOR:

•Sandwiched Region: N-Type region is sandwiched b/w two P-Type Regions.

•Biasing: Forward biased voltage at emitter-base junction VBB will shif electron holes from emitter to base region which are swept towards collector region due to large reverse biased voltage Vcc.



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Q NO 5: N-TYPE MATERIAL || P-TYPE MATERIAL

(i) Doping

N-Type	P-Type
→ Pure semiconductor doped w/ **pentavalent impurity** like Phosphorous	→ Pure semiconductor doped w/ **trivalent impurity** like Boron

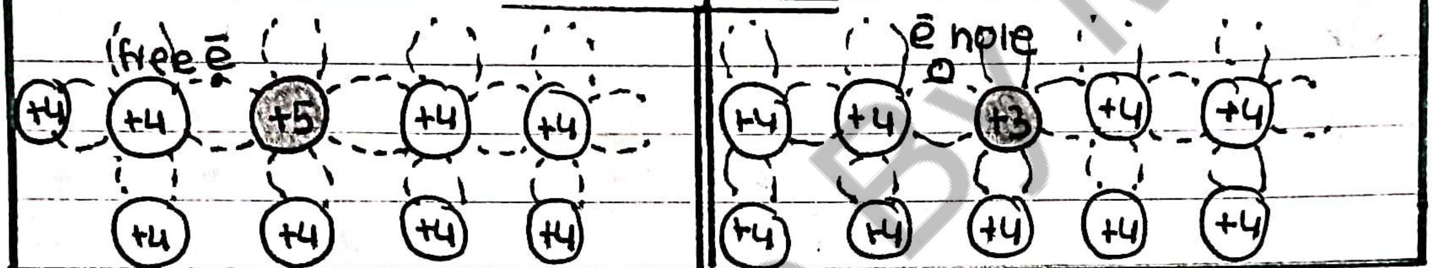
(ii) Role of Impurity Atoms

N-Type	P-Type
→ Impurity atom acts like **donor**	→ Impurity atoms act like **acceptors**

(iii) Majority Carriers

N-Type	P-Type
→ **Negative charge carriers** or electrons are majority carriers	→ **Positive charge carriers** or electron holes are majority carriers

(iv) Diagram



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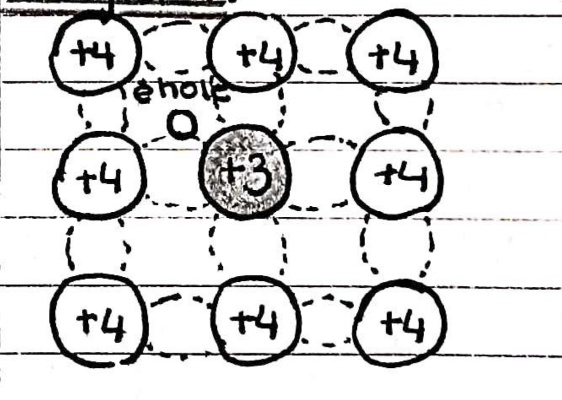
Q NO 6: → NEUTRAL NATURE OF P-TYPE SEMICONDUCTOR:

A P-Type semiconductor is obtained as a result of doping trivalent impurity like Boron belonging to group III.

Diagram:



• **Neutral pure semiconductor atoms:** Semiconductor atoms are **electrically neutral**

• **Neutral impurity atoms:** The impurity added is also **electrically neutral**

• **Over all effect:** As impurity and pure semiconductor atoms are neutral, P-Type material is also neutral

→ **CONCLUSION:** Thus P-Type material can be negatively charged only if its hole gain electrons from external source

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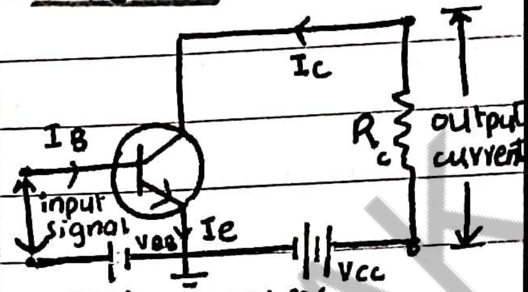
QNO 7: Common emitter configuration is preferred as compared to common base and common collector because;

→REASONS

(i) High input impedance: common emitter mode has high input impedance and low output impedance

Diagram:



NPN transistor

(ii) High voltage and current gain: CE mode has high current and voltage gain

(iii) High power gain: CE mode has very high power gain

(iv) Stable output signal: CE mode has most stable signal at output.

→MATHEMATICALLY: current gain $\beta = I_C / I_B$

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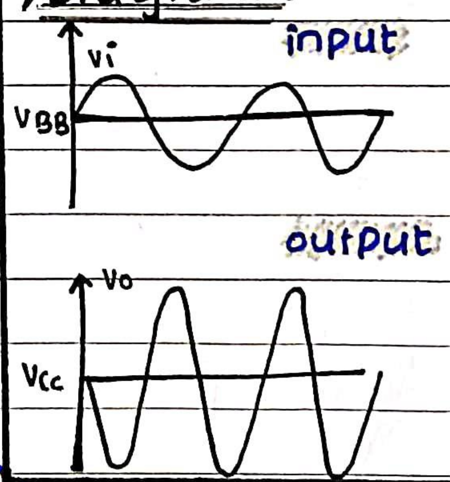
QNO8: →TRANSISTOR AS AN AMPLIFIER: Common Emitter (CE) configuration is commonly used for amplification.

• **current gain:** Signal to be amplified is provided between base and emitter, it will change input base current. In other words we can say that input signal adds up with 'VBE' and emitter along with base current increase causing collector current to increase developing an amplified output signal.

→Diagram:



→Mathematically: $\beta_{gain} = I_C / I_B$

gain of amplifier, $\frac{\Delta V}{\Delta V_{in}} = -\beta \frac{R_C}{R_i}$

Q.No.9: → **GIVEN:** silicon atoms = 10^{10}

trivalent atoms = 10

Temprature = 25°C

→ **REQUIRED:** free electrons = ? ①

electron holes = ? ②

→ **SOLUTION:**

① we know that 1 trivalent impurity = 1 electron hole

thus 10 trivalent atoms = 10 electron holes

② Due to doping no free electrons will be generated but at 25°C some electrons break their covalent bonds due to thermal effect and electron holes also appear

→ **RESULT:** Total number of charge carriers will be 10 holes + holes created due to thermal effect corresponding to equal number of free electrons.

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